## **REMARKS**

In the Office Action dated March 25, 2005, claims 1-48 were rejected under 35 U.S.C. § 103 over U.S. Patent No. 6,182,136 (Ramanathan) in view of U.S. Patent No. 5,490,252 (Macera).

Applicant respectfully notes that the Office Action is incomplete, as no rejection or indication of allowability was provided with respect to claims 49-52. In view of the lack of any rejections of claims 49-52, allowance of claims 49-52 is respectfully requested.

It is respectfully submitted that a *prima facie* case of obviousness has not been established with respect to independent claim 1 for at least the following reasons: (1) no motivation or suggestion existed to combine the teachings of Ramanathan and Macera; and (2) even if combined, the hypothetical combination of Ramanathan and Macera does not teach or suggest all elements of the claims. *See* M.P.E.P. § 2143 (8<sup>th</sup> ed., Rev. 2), at 2100-129.

With respect to claim 1, the Office Action conceded that Ramanathan fails to disclose selecting an IP route from the set of routes which meets predetermined criteria. 3/25/2005 Office Action at 3. However, the Office Action relied upon Macera as teaching the missing element.

Applicant respectfully submits that Macera does not teach or suggest selecting an IP route from a set of routes which meets predetermined criteria. Macera describes an inter-networking system for exchanging packets of information between networks, such as among an Ethernet network, an FDDI network, a token ring network, a T1/E1 network, and a DS3 network, as depicted in Fig. 3. Macera, 1:66-2:1. The inter-networking system described in Macera is a broadband enterprise switch (BES), referred to as a high-performance, high-availability switch by Macera. Macera, 3:66-4:4. As depicted in Fig. 3, the BES of Macera includes a system bus 43 that is connected to various interface modules (labeled 78, 80, 82, 84, and 86 in Fig. 3). With the arrangement depicted in Fig. 3, the BES can be used to interconnect the various networks illustrated in Fig. 3. See, e.g., Macera, 5:29-33. A data packet flow for the BES architecture depicted in Fig. 3 is described in column 20 of Macera. In the example described in Macera, LAN packets are received by the Ethernet interface module 78 of Fig. 3. Macera, 20:43-45. The packets are then sent to the system bus 43 to an FPSE 62 where a copy of the packet is stored in a central buffer 56. Macera, 20:47-50. A filter 218 examines the source address of the packet to determine if the source address has been seen

The following prior art references have been cited in the International Search Report and copies are enclosed:

- 1. WO 0110090
- 2. WO 9817042
- 3. WO 9638987
- 4. WO 9908424
- 5. US 5553145
- 6. Articles:
  - A. Author Giorgio Cevenini, et al.; Entitled "A MultiProvider, Universal, E-Mail Service for the Secure Exchange of Legally-Binding Multimedia Documents;" Dated May 2000; Entire Document.
  - B. Author IBM Technical Disclosure Bulletin, IBM Corp., New York, U.S.; Entitled "Method for Automated Communication to Third Parties Upon Composite Acknowledgement"; Dated February 1, 1994; Pages 345-346.
  - C. Author K. Moore, University of Tennessee; Entitled "An Extensible Message Format for Delivery Status Notifications";
    Dated January 1996; Page 6, Line 27 to Page 7, Line 33; Page 14, Line 28 to Page 20, Line 34.

Because this Information Disclosure Statement is filed prior to the first Office action on the merits, no fee is required. The Commissioner is authorized, however, to charge any fees that may be required by this paper to Deposit Account No. 06-2425. A duplicate copy of this paper is enclosed.

Applicant respectfully requests that the foregoing citations be considered and made of record. It is respectfully requested that the examiner indicate consideration of the cited references by returning a copy of the attached form PTO/SB/08A with initials and/or other appropriate marks.

Respectfully submitted, FULWIDER PATTON LEE & UTECHT, LLP

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